REMARKS

Favorable reconsideration of this application is respectfully requested.

Claims 1, 3-12, and 15-19 are pending in this application. Claims 1, 3-12 and 15-19 were rejected under 35 U.S.C. § 112, second paragraph. The drawings were objected to. Claims 1, 2, 5, 13, and 14 were rejected under 35 U.S.C. § 102(b) as anticipated by JP 11-178216 to Keizo et al. (herein "Keizo"). Claims 3, 7, and 12, 18, and 19 were rejected under 35 U.S.C. § 103(a) as unpatentable over Keizo in view of U.S. Patent 6,753,622 to Oughton, JR. (herein "Oughton"). Claim 4 was rejected under 35 U.S.C. § 103(a) as unpatentable over Keizo, in view of U.S. Patent 5,866,506 to Ozawa.[1] Claim 6 was rejected under 35 U.S.C. § 103(a) as unpatentable over Keizo in view of U.S. Patent 6,034,514 to Sakai. Claim 15 was rejected under 35 U.S.C. § 103(a) as unpatentable over Keizo in view of the publication ("Improved single-phase line-interactive UPS") to Bong-Hwan et al. (herein "Bong-Hwan"). Claims 8-11 and 16 were rejected under 35 U.S.C. § 103(a) as unpatentable over Keizo in view of U.S. Patent 5,786,992 to Vinciarelli et al. (herein "Vinciarelli"). The above-noted rejections are traversed by the present response as now discussed.

Addressing first the rejection of claims 1, 3-12, and 15-19 under 35 U.S.C. § 112, second paragraph, that rejection is traversed by the present response.

The above-noted grounds for rejection indicates the use of the terms "series" and "parallel" in the claims is not clear. Applicants traverse that position and submit the claims properly use those terms. In fact applicants submit the claims recite a structure consistent with the noted interpretation of the term "series" and "parallel" on page 3 of the Office Action. Page 3 of the Office Action indicates a "series" connection is one where components

[1] With respect to that rejection of claim 4, applicants note the outstanding rejection cites Ozawa as U.S. Patent 5,866,506. However, U.S. Patent 5,866,506 is not a patent to Ozawa but instead to Tutt et al., and the disclosure in Tutt does not appear at all related to the claimed features, and does not include even a Figure 5B as cited in Ozawa. It appears the Office Action has cited the incorrect reference, and clarification of that basis for the rejection is respectfully requested. This request was previously also made but was not addressed.

share the same current, and a "parallel" connection is one in which components share the same voltage.

Independent claim 1 as an example recites a straightforward switch connected in series between a power source and a load. As shown in Figure 1 of the present specification as a non-limiting example, an annoted version of which is provided below, applicants submit the switch 3 does "share the same current" as the power source 1 and the load 2, see the "series line" in the below figure. Independent claim 1 also recites the first single-phase inverter/rectifier is connected in parallel with the series connection of the power source and the straightforward switch and now clarifies the second single phase inverter/rectifier is connected in series with the load. As shown in the below figure, and as is also clear from Figure 6-8 and 15-18, every second inverter or rectifier 5 is connected in series with the load 2 from the power source 1 as shown by the solid "series line", and every first inverter or rectifier 4 is connected in parallel with the load 2 from the power source as shown in the dotted "parallel lines". Applicants thereby submit usage of the terms "series" and "parallel" in the claims clearly proper given the noted definition of parallel connection as sharing a same voltage.

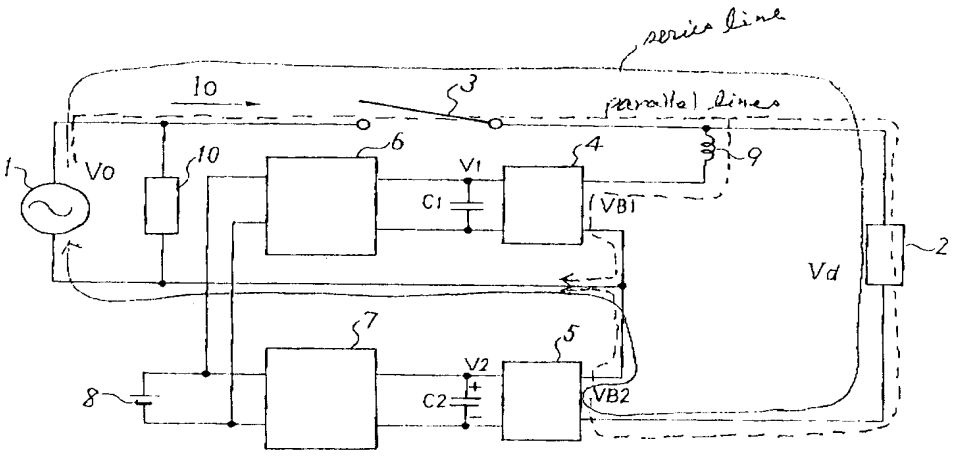

Fig. 1

Independent claim 1 further recites the first and second single phase inverters/rectifiers are connected to be in series with each other ***when the straightforward***

switch is open. Applicants submit the outstanding rejection does not appear to fully consider that claim language, which requires a series connection between the inverter/rectifiers 4, 5 ***when the switch 3 is open***. In that situation applicants submit the rectifiers 4, 5 are in series.

Thereby, applicants respectfully submit the terms "series" and "parallel" are properly used in the claims.

The outstanding rejection also indicated the term "inverter/rectifier" was confusing. In reply to that statement each of the claims no longer recites the term "inverter/rectifier", but now instead recites "inverter or rectifier".

The claims are also amended so that the switch is no longer referred to as on, but instead "open".

Independent Claims 1 and 12 also no longer recite the term "superimposing".

With regard to the rejection of claims 5 and 19 as reciting the term "pseudo-sinusoidal voltage wave", applicants submit that term is clear in view of the specification, and thus definite to one of ordinary skill in the art.

More particularly, the specification shows for example in Figures 2(a) and 2(b) how a pseudo-sinusoidal voltage wave is generated, and that subject matter is also clearly discussed in the specification at page 7, paragraph [0013]. Also provided with the present response as an Attachment is a publication that also explains a "pseudo-sinusoidal voltage wave", which applicants submit provides further evidence that such a term would had been understood by one of ordinary skill in the art. In view of such disclosures, applicants respectfully submit the claim term "pseudo-sinusoidal voltage wave" is clear to one of ordinary skill in the art.

In view of the presently submitted claim amendments and foregoing comments, applicants respectfully submit each of the pending claims is proper under 35 U.S.C. § 112, second paragraph.

Addressing now the objection to the drawings, the drawings were objected to based as the use of terms "series" and "parallel" in the claims not being clearly shown in the drawings. As noted above, applicants submit the claims are proper in reciting the terms "series" and "parallel", and thereby the drawings are believed to be proper.

Addressing the above-noted prior art rejections, the claims as currently written are believe to distinguish over the applied art.

Initially applicants note the claims are amended to clarify features recited therein. Independent claim 1 now further recites:

> wherein said first and second single phase inverter or rectifier are connected so as to be connected in series with each other when said straightforward switch is open to thereby each supply their respective electric powers to the load by each supplying their respective output voltages to the load.

Applicants respectfully submit such claim features are not taught or suggested by the applied art.

According to features recited in independent claim 1, and with reference to Figure 1 in the present specification as a non-limiting example, a first single phase inverter/rectifier 4 is connected in parallel with a power source 1. Further, first and second single phase inverters or rectifiers 4, 5 are connected so as to be connected in series with each other when the switch 3 is open, so that each of those inverters or rectifiers 4 and 5 supply electric power to the load 2 by each supplying their respective output voltages to the load 2.

Each outstanding rejection cites Keizo as the primary reference. However, in contrast to the claimed features in Keizo the noted first inverter 6 is ***not connected in parallel*** with a series connection of the power source 1 and the switch 2. Keizo itself specifically states in the Abstract "... a second converter 6 the switch of which is connected in ***series*** with the power source 1 together with its AC output side..." (emphasis added).

Moreover, applicants respectfully submit Keizo further does not disclose or suggest the claimed "first and second single phase inverters or rectifiers are connected so as to be connected in series with each other when the straightforward switch is open to thereby each supply their respective elective power to the load by each supplying their respective output voltages to the load". In contrast to that claimed feature in Keizo only the first converter 4 supplies its output voltage to the load 3 when the switch 2 is turned off.

In view of the foregoing comments, applicants respectfully submit amended independent claim 1, and thereby the claims dependent therefrom, patentably distinguish over Keizo.

Moreover, no disclosures in any of the further recited references to Oughton, Ozawa, Sakai, Bong-Hwan, or Vinciarelli were cited with respect to the above-noted features, and no further disclosures in any of those other cited references are believed to cure the above-noted deficiencies of Keizo with respect to independent Claim 1.

With respect to independent claim 18, independent claim 18 recites:

> a first single phase inverter or rectifier connected in parallel with the series connection of the power source and the straightforward switch;

As discussed above, Keizo does not disclose or suggest such a feature.

Further, independent claim 18 is herein amended by the present response to clarify:

> a DC-DC converter connected between the battery and at least one of said first and second single phase inverters or rectifiers, wherein the first and second single phase inverters or rectifiers generate output voltages different from each other and are connected so that each of their output voltages are applied to the load when the straightforward switch is open.

Applicants respectfully submit the above-noted features are neither taught nor suggest by Keizo in view of Oughton. As noted above, Keizo does not disclose or suggest outputs from both of the noted rectifiers 4 and 6 being applied to the load 3 when the switch 2 is

open. Instead in Keizo only the first converter 4 supplies its voltage to the load 3 when the switch 2 is open. Moreover, no discloses in Oughton cure that deficiency in Keizo.

In view of foregoing comments, applicants respectfully submit amended independent claim 18, and accordingly the claims dependent therefrom, patentably distinguish over Keizo, and further in view of Oughton.

Moreover, no disclosures in any of the further cited references to Ozawa, Sakai, Bong-Hwan, or Vinciarelli were cited with respect to the above-noted features in independent claim 18, and no disclosures in those further references are believed to cure the above-noted deficiencies of Keizo in view of Oughton.

In view of the foregoing comments applicants respectfully submit each of amended independent claims 1 and 18, and accordingly the claims dependent therefrom, positively recite features neither taught nor suggested by the applied art, and thus are allowable over the applied art.

As no other issues are pending in this application, it is respectfully submitted that the present application is now in condition for allowance, and it is hereby respectfully requested that this case be passed to issue.

Respectfully submitted,

OBLON, SPIVAK, McCLELLAND,
MAIER & NEUSTADT, P.C.

Customer Number
22850

Tel: (703) 413-3000
Fax: (703) 413 -2220
(OSMMN 06/04)

Gregory J. Maier
Attorney of Record
Registration No. 25,599

Surinder Sachar
Registration No. 34,423

GJM\SNS

A Circular Voltage-Controlled Phase Shifter with Unlimited Phase Range for Phase Tracking Loops

Byungjin Chun, Zheyao Zhang, and Sverre Lidholm
Department of Microelectronic Engineering
University College Cork, Ireland
bchun@ue.ucc.ie

***Abstract*—A circular voltage-controlled phase shifter (VCPS) is proposed to extend the range of the controlled output phase shift unlimitedly. This is made possible by configuring the system to operate in a circular way, differently from the conventional VCPS whose output phase saturates as the phase control input exceeds some value. The circular VCPS is based on a vector modulation method whose modulation signals are generated in a pseudo-sinusoidal way exploiting the current-voltage (I-V) curve of a MOS differential amplifier pair. When the circular VCPS is employed in phase tracking loops, the loop can operate in a stand-alone way thanks to its unlimited phase shifting capability.**

I. Introduction

The voltage-controlled phase shifter (VCPS) is often used in electronic devices like phase-locked loop (PLL), delay-locked loop (DLL) and other phase controlling systems. In particular, there have been several attempts to apply a VCPS to multiple antenna receivers or beamformers [1] [2].

A common problem that they have is that their variable range of the output phase is limited to some value. When a phase control system (e.g., PLL) operates in an autonomous way, the control voltage may exceed a value corresponding to the maximum phase shift during operation. Without any other means, the control system is highly likely to be stuck at a phase shift boundary. Because of this problem, the above beamformers employ data converters and a digital baseband signal processor so that the VCPS is provided with the phase information, which is confined within a finite range, by the baseband signal processor. Obviously, this makes the system complex. Instead, it is quite desirable to design the phase control system so that it can operate in a stand-alone way in the analogue domain. This can be achieved by employing a VCPS which works in a *circular* way, as is described in this paper.

An example of a VCPS with unlimited phase range is found in [3]. The [3] carries out a circular operation to achieve unlimited output phase range. However, it is basically designed for phase shifting of digital signals in DLL, whereas the proposed VCPS is for phase shifting of analogue signals with arbitrary phase modulation. This paper shows how the concept of the circularity can be applied to extend the phase shifting range of analogue signals indefinitely by exploiting the current-voltage (I-V) curve of a MOS differential amplifier pair.

In Section II, we describe the operation and implementation of the proposed circular VCPS, and in Section III, simulation results and discussions are given. Finally, a conclusion is given in the last section.

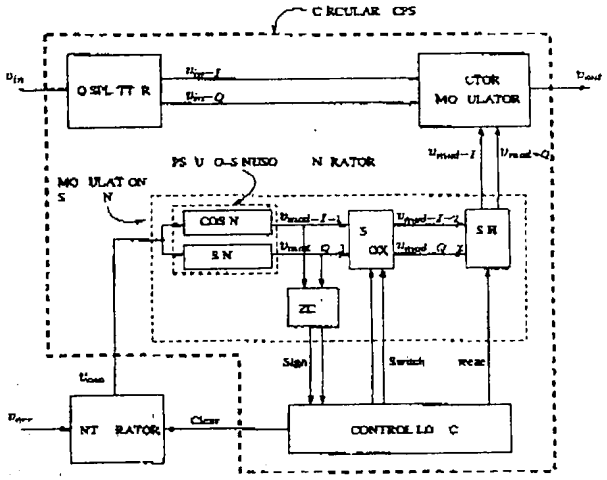

Fig. 1. Block diagram of the proposed circular VCPS in association with an integrator.

II. Proposed Circular VCPS

We explain the proposed circular VCPS in association with an integrator (see Fig. 1) since this configuration is a typical building block in many phase tracking loops. The integrator accumulates a phase error signal from the phase detector in the phase tracking loop and provides a phase control signal for the VCPS.

A. Overall Operation

Let the RF input signal be represented as

$$v_{in}(t) = A\sin\{2\pi f_c t + \theta(t)\} \quad (1)$$

where A, f_c and $\theta(t)$ are the amplitude, centre frequency and phase modulation, if any, of the signal. Then, the RF ouput signal v_{out} should be a phase-shifted version of v_{in} as commanded by the control signal v_{con}. That is,

$$v_{out}(t) = A\sin\{2\pi f_c t + \theta(t) + \phi(v_{con})\} \quad (2)$$

where $\phi(v_{con})$ is the desired phase shift as a function of v_{con}. We assume $A = 1$ for convenience and $\phi(v_{con}) = \frac{\phi_0}{v_0} v_{con}$ so that $\phi(v_0) = \phi_0$, $\phi(0) = 0$ and $\phi(-v_0) = -\phi_0$.

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To implement $v_{out}(t)$ as expressed in (2), we analyse this expression using a trigonometric equality as

$$v_{out}(t) = \sin\{2\pi f_c t + \theta(t)\} \cdot \cos\{\phi(v_{con})\} + \cos\{2\pi f_c t + \theta(t)\} \cdot \sin\{\phi(v_{con})\}. \quad (3)$$

From (3), we can see that $v_{out}(t)$ can be obtained through the following steps: First, generate a quadrature pair of the RF input signal such as $v_{in\_I}(t) = \sin\{2\pi f_c t + \theta(t)\}$ and $v_{in-Q}(t) = \cos\{2\pi f_c t + \theta(t)\}$. Second, generate a quadrature pair of modulation signals such as $v_{mod-I}(v_{con}) = \cos\{\phi(v_{con})\}$ and $v_{mod-Q}(v_{con}) = \sin\{\phi(v_{con})\}$ as a function of v_{con}. Finally, vector-modulate the two quadrature pairs to generate the RF output signal as indicated in (3).

The v_{in-I} and v_{in-Q} can be generated using a wideband in-phase and quadrature (IQ) splitter reported in [4], and the vector modulation can be easily realised employing well-known Gilbert cells. The major problem here is how to generate the modulation signal pair v_{mod-I} and v_{mod-Q} in an analogue circuit. The method employed in this paper is to generate a pseudo-sinusoidal waveform pair for a finite range (i.e., $-v_0 \le v_{con} \le v_0$), which approximates the true sinusoidal waveforms for the range, and manipulate the waveforms in such a way that an unlimited range of v_{con} or, equivalently, an unlimited phase shifting range can be covered.

B. Modulation Signal Generator

An example of the pseudo-sinusoidal waveforms (denoted $v_{mod-I-1}$ and $v_{mod-Q-1}$) are shown in Fig. 2 (A) and (B) in solid curves. They resemble the true cosine and sine waveforms in a finite range of the phase control signal (i.e., $-v_0 \le v_{con} \le v_0$). As a result, when these waveforms are directly applied to the modulation signal ports of the vector modulator in Fig. 1, it will shift the phase of v_{in} from $-\phi_0$ to ϕ_0 as v_{con} varies from $-v_0$ to v_0 as shown in Fig. 2 (C). However, they will be saturated at a certain value as soon as v_{con} goes beyond either boundary point, not being extended in a sinusoidal fashion. As a solution for that, we choose to switch the pseudo-sinusoidal waveforms when v_{con} crosses over either boundary point so that the phase shifting characteristic repeats the previous curve. This operation is called the phase domain change in this paper, and is commanded by the Switch signal from the control logic.

As a typical example, we divide the whole phase range into four overlapping phase domains: D1 ($-90°$ to $90°$), D2 ($0°$ to $180°$), D3 ($90°$ to $270°$), D4 ($-180°$ to $0°$) with $\phi_0 = 90°$. They overlap with the neighbouring phase domains in order to achieve a hysterisis characteristic. This can avoid a bouncing problem between the phase domains when v_{con} crosses the boundary. Actually, [3] did not consider the hysterisis. The Fig. 3 (A)-(D) describes the required modulation signals (denoted $v_{mod-I-2}$ (solid) and $v_{mod-Q-2}$ (dashed)) for the phase domains D1-D4, respectively. Let us initialize the operation at $v_{con} = 0$ (indicated (a') in Fig. 3 (A)). In D1, $v_{mod-I-2}$ is set to $\cos(\frac{\phi_0}{v_0} v_{con})$ and $v_{mod-Q-2}$ is set to $\sin(\frac{\phi_0}{v_0} v_{con})$. As v_{con} increases to reach v_0 (indicated (b)), the phase domain should be changed from D1 to D2 with $v_{mod-I-2}$ switched to $-\sin(\frac{\phi_0}{v_0} v_{con})$, $v_{mod-Q-2}$ switched to $\cos(\frac{\phi_0}{v_0} v_{con})$ and v_{con} reset to zero (indicated (b')). This is triggered by detecting the zero-crossing point of $v_{mod-I-1}$ and sending the Sign signal to the control

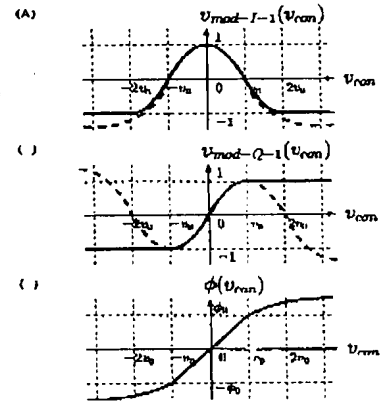

Fig. 2. Transfer curves of (A) $v_{mod-I-1}$ (solid), (B) $v_{mod-Q-1}$ (solid) and (C) output phase shift as a function of v_{con}, respectively. The dashed curves in (A) and (B) indicate the synthesised pseudo-sinusoids according to (7) and (8) in the case of $v_0 \neq V_Q$.

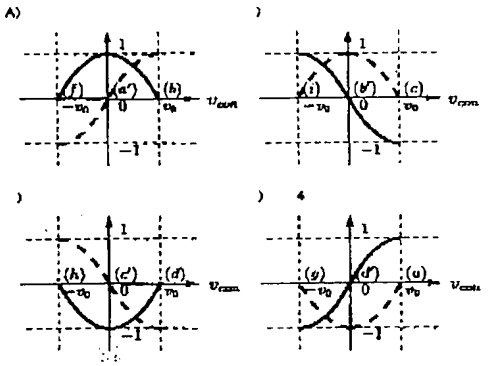

Fig. 3. Modulation signal pair $v_{mod-I-2}$ (solid) and $v_{mod-Q-2}$ (dashed) for the respective phase domains D1-D4.

logic. Then, the control logic switches the pseudo-sinusoidal waveforms and clears the integrator by activating the Switch and the Clear signals, respectively. The above operation turns around (A) to (D) and repeats as v_{con} keeps on increasing. In the same way, the pseudo-sinusoidal waveforms can be continued unlimitedly in the negative direction as v_{con} decreases.

However, because of a finite time in clearing the integrator and in switching the pseudo-sinusoidal waveforms, the phase shifted version would be venerable to switching glitches during the phase domain change. To solve this problem, we put a *clutching* block between the switch box and the vector modulator. The clutching block disconnects the path between the two blocks temporarily while changing the phase domain in order to keep the last modulation signals v_{mod-I} and v_{mod-Q} undisturbed. The clutching block is realised by using a sample and hold circuit under the control of the Freeze signal from the control logic.

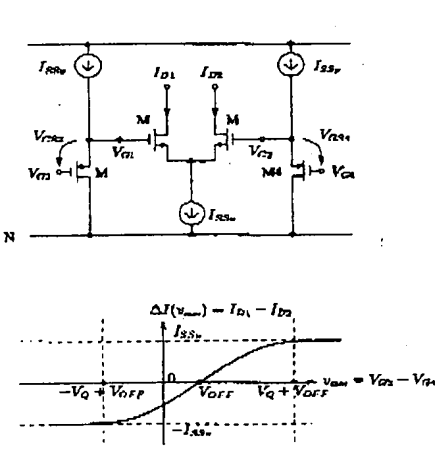

Fig. 4. (A) MOS differential amplifier pair with input voltage offset, and (B) its I-V curve.

C. PSUEDO-SINUSOIDAL WAVEFORM GENERATOR

One of the novelties of the paper is the pseudo-sinusoidal waveform generator. By superimposing several I-V curves of a MOS differential amplifier pair, desired pseudo-sinusoidal waveforms can be synthesised for a finite control input range. We consider a MOS differential amplifier pair shown in Fig. 4 (A). Assuming the gate voltage V_{G1}, V_{G2} and the drain current I_{D1}, I_{D2} of M1 and M2, respectively, its transfer curve between the differential voltage input $v_{con} = V_{G1} - V_{G2}$ and the differential current output $\Delta I(v_{con}) = I_{D1} - I_{D2}$ is given by [5]

$$\Delta I(v_{con}) = \begin{cases} \frac{1}{2}K_n\left(\frac{W}{L}\right)_1 v_{con}\sqrt{\frac{4I_{SSn}}{K_n\left(\frac{W}{L}\right)_1} - v_{con}^2}, \\ \qquad -V_Q \le v_{con} \le V_Q, \\ I_{SSn}, \quad v_{con} \ge V_Q, \\ -I_{SSn}, \quad v_{con} \le -V_Q \end{cases} \tag{4}$$

where $V_Q = \sqrt{\frac{2I_{SSn}}{K_n\left(\frac{W}{L}\right)_1}}$ is the saturation voltage for v_{con}, and I_{SSn} is the source bias current of the MOS pair, K_n is the N-MOS transconductance parameter, and $\left(\frac{W}{L}\right)_1 = \left(\frac{W}{L}\right)_2$ is the aspect ratio of M1 and M2, respectively. Note that the transfer curve as depicted in Fig. 4 (B) resembles a portion of the true sine curve for $-V_Q \le v_{con} \le V_Q$ with $V_{OFF} \simeq 0$. However, its mathematical form given in (4) is obviously different from the true sine curve. We may improve the approximation to the true sine curve by employing multiple differential amplifier pairs [6].

The offset version $\Delta I(v_{con} - V_{OFF})$ of the basic I-V curve can be realised by adding two source followers M3, M4 with different gate-source voltage drops V_{GS3}, V_{GS4} to M1 and M2, respectively. The offset voltage $V_{OFF} = |V_{GS4}| - |V_{GS3}|$ can be adjusted by varying $\left(\frac{W}{L}\right)_3$ and $\left(\frac{W}{L}\right)_4$ of M3 and M4. That is, using the relationship $|V_{GS3}| = V_{THp} + \sqrt{\frac{2I_{SSp}}{K_p\left(\frac{W}{L}\right)_3}}$ and $|V_{GS4}| = V_{THp} + \sqrt{\frac{2I_{SSp}}{K_p\left(\frac{W}{L}\right)_4}}$, we get $V_{OFF} = \sqrt{\frac{2I_{SSp}}{K_p}}\left(\frac{1}{\sqrt{\left(\frac{W}{L}\right)_4}} - \frac{1}{\sqrt{\left(\frac{W}{L}\right)_3}}\right)$. Here, V_{THp} and I_{SSp} are the threshold voltage of the P-MOS transistor and its source bias current, respectively. Then, by putting

$$\left(\frac{W}{L}\right)_4 = \frac{1}{(N+1)^2}\left(\frac{W}{L}\right)_3 \tag{5}$$

for an integer N, we get

$$V_{OFF} = Nv_0 \tag{6}$$

for a reference voltage $v_0 = \sqrt{\frac{2I_{SSp}}{K_p\left(\frac{W}{L}\right)_3}}$.

Then, using (4) and (6) with $v_0 \approx V_Q$, the desired waveforms for $v_{mod-I-1}$ and $v_{mod-Q-1}$ in Fig. 2 (A) and (B) (solid) can be synthesised for $-v_0 \le v_{con} \le v_0$ according to

$$v_{mod-I-1}(v_{con}) = \{\Delta I(v_{con} + v_0) - I_{SSn} - \Delta I(v_{con} - v_0)\} R_L, \tag{7}$$

$$v_{mod-Q-1}(v_{con}) = \{-\Delta I(v_{con} + 2v_0) + \Delta I(v_{con}) - \Delta I(v_{con} - 2v_0)\} R_L \tag{8}$$

with a load resistance R_L. They are shown in Fig. 2 (A) and (B) in dashed curves, respectively. Note that, in (8), two extra terms $-\Delta I(v_{con} + 2v_0)$ and $-\Delta I(v_{con} - 2v_0)$ are added to $\Delta I(v_{con})$ which is originally needed. This is to make sure that the pseudo-sinuoidal waveform pair maintain the quadrature relationship in $-v_0 \le v_{con} \le v_0$ in spite of potential mismatch between v_0 and V_Q. This effect can be seen from the following argument. If the pair maintains the quadrature relationship in the range, the $\mp 90°$ phase offset versions of $v_{mod-Q-1}(v_{con})$, which are $v_{mod-Q-1}(v_{con} + v_0)$ and $v_{mod-Q-1}(v_{con} - v_0)$, should be equal to $v_{mod-I-1}(v_{con})$ for $-v_0 \le v_{con} \le 0$ and $-v_{mod-I-1}(v_{con})$ for $0 \le v_{con} \le v_0$, respectively (see Fig. 2 (A) and (B)). Without the extra terms, unless v_0 and V_Q are well matched, $v_{mod-Q-1}(v_{con}+v_0)$ and $v_{mod-Q-1}(v_{con}-v_0)$ in (8) would be considerably different from $v_{mod-I-1}(v_{con})$ and $-v_{mod-I-1}(v_{con})$ in (7) as v_{con} approaches 0. On the contrary, with the extra terms, we have $v_{mod-Q-1}(v_{con}+v_0) = \{-\Delta I(v_{con}+3v_0) + \Delta I(v_{con}+v_0) - \Delta I(v_{con}-v_0)\} R_L \approx v_{mod-I-1}(v_{con})$ since $\Delta I(v_{con}+3v_0) \approx I_{SSn}$ for $-v_0 \le v_{con} \le v_0$. Similarly, we have $v_{mod-Q-1}(v_{con} - v_0) \approx -v_{mod-I-1}(v_{con})$ for $-v_0 \le v_{con} \le v_0$.

Schematics of the pseudo-sinusoidal waveform generator based on (7) and (8) are shown in Fig. 5 (A) and (B), respectively. It is implemented with fully differential mode in $3.3V$ $0.35\mu m$ CMOS technology. In the circuit, $\left(\frac{W}{L}\right)_1$-$\left(\frac{W}{L}\right)_{10}$ for the basic MOS pairs are set to $\left(\frac{30}{0.35}\right)$ alike. And, $\left(\frac{W}{L}\right)_{11}$-$\left(\frac{W}{L}\right)_{14}$ are set to $\frac{2}{0.35}$, $\frac{8.8}{0.35}$, $\frac{8.8}{0.35}$, $\frac{2}{0.35}$ with $V_{OFF} = -v_0, v_0$ [1], and $\left(\frac{W}{L}\right)_{15}$-$\left(\frac{W}{L}\right)_{20}$ are set to $\frac{1}{0.35}$, $\frac{8}{0.35}$, $\frac{9}{0.35}$, $\frac{9}{0.35}$, $\frac{8}{0.35}$, $\frac{1}{0.35}$ with $V_{OFF} = -2v_0, 0, 2v_0$, respectively, according to (5) and (6). The I_{SSn} and I_{SSp} are fixed to 60 and 10 μA, respectively. The R_L is set to 3.4 $K\Omega$ alike.

III. SIMULATION RESULTS AND DISCUSSIONS

To show the performance of the proposed circular VCPS, a testbed is set up according to Fig. 1. A constant phase error signal $v_{ERR} = V_{DD}$ is applied to the integrator. A switched

[1]The $\left(\frac{W}{L}\right)$'s are tuned from initial values $\frac{2}{0.35}$, $\frac{8}{0.35}$, $\frac{8}{0.35}$, $\frac{2}{0.35}$.

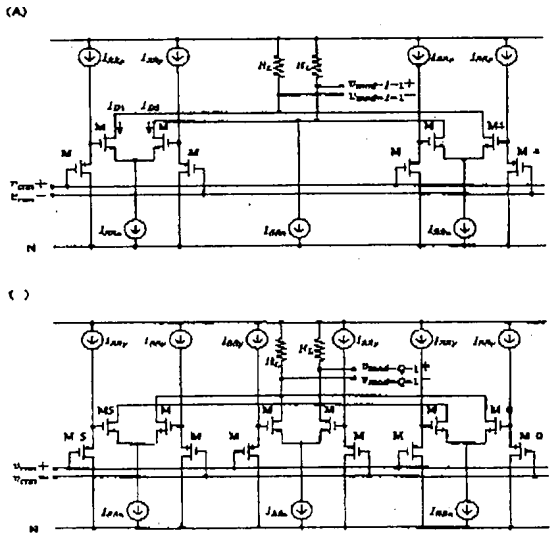

Fig. 5. (A) Pseudo-cosine ($v_{mod-I-1}$) and (B) Pseudo-sine ($v_{mod-Q-1}$) waveform generators.

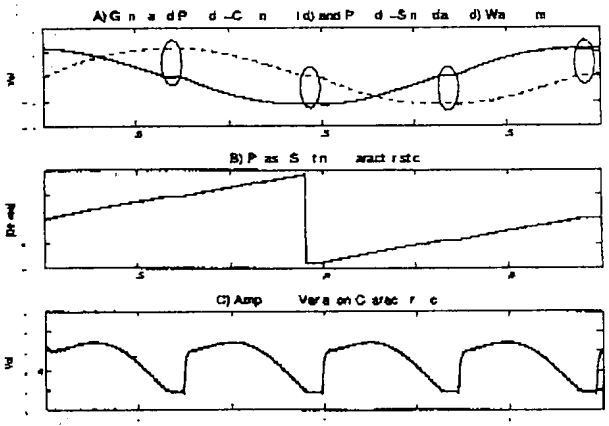

Fig. 6. (A) Generated pseudo-cosine (v_{mod-I}) and pseudo-sine (v_{mod-Q}) waveforms, (B) Phase shifting characteristic, (C) Amplitude variation characteristic. Here, a constant positive phase error signal is applied to the integrator so that the VCPS covers the full phase domains. The ovals in (A) indicate the phase domain change period.

capacitance-type integrator is employed considering precise component value matching. In other words, it is easier to realise a precise proportionality constant of the integrator by matching relative capacitance values than the RC-type integrator whose proportionality constant depends on the absolute R and C values. The employed switching frequency is 50 MHz.

The simulated waveforms for v_{mod-I} and v_{mod-Q} (not $v_{mod-I-1}$ and $v_{mod-Q-1}$) are shown in Fig. 6 (A). We can see that the desired pseudo-sinusoidal waveforms are generated as the time elapses as a result of application of the positive v_{err}. This corresponds to the waveforms for $v_{con} > 0$ in Fig. 3 (A). When either v_{mod-I} or v_{mod-Q} crosses zero, the phase domain change takes place with clearing the integrator output. This process repeats and the whole phase domains from D1 to D4 are covered.

The phase and amplitude of the output signal v_{out}, which are determined by $tan^{-1}(\frac{v_{mod-Q}}{v_{mod-I}})$ and $\sqrt{v_{mod-I}^2 + v_{mod-Q}^2}$, are plotted in Fig. 6 (B) and (C), respectively. From the plot, we can see that the unlimited phase shifting is achived in a circular way (except during the phase domain change period), and the phase shifting is almost linear in the normal intervals. The maximum phase deviation from the linear slope due to the non-ideality of the pseudo-sinusoids is measured to be 3.5°. At the same time, the maximum amplitude deviation ratio from the constant envelope is measured to be 2.2 percent.

Meanwhile, the VCPS is insensitive to v_{err} during the phase domain change period, which is fixed as 5 clock cycles (100 ns) here. However, this is not a serious problem in usual applications. For example, if it is applied to a phase tracking loop in 802.11a-based WLAN, the period is very short in the light of the actual phase variation rate of the typical wireless fading channels or the preamble period of 16 μs which is provided for synchronisations.

IV. Conclusions

A circular VCPS with unlimited phase range was proposed and implemented in the analogue CMOS circuit. To achieve the unlimited phase range, methods of generating pseudo-sinusidal waveforms and of achieving the circularity were presented. Besides the unlimited phase range, the simulation results of the proposed VCPS showed small phase deviation (3.5°) and amplitude deviation (2.2 percent) from the ideal phase shifter. Therefore, the proposed VCPS is considered suitable for stand-alone analogue phase tracking loop applications.

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